AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data driving apparatus for a liquid crystal display device, comprising:

a first multiplexer part performing a time-division on inputted digital pixel data;

a digital-analog converter part converting the time-divided digital pixel data from the first multiplexer part to analog pixel signals;

a demultiplexer part separately supplying the analog pixel signals from the digital-analog converter part to a plurality of output channels, respectively during the first half of a horizontal period and during the second half of the horizontal period; and

an output part outputting simultaneously the analog pixel signals from the corresponding demultiplexer output channels to corresponding data lines[[,]],

wherein the output part comprises:

a sampling part sampling the pixel signals from the demultiplexer output channels;

a capacitor part holding the sampled pixel signals from the sampling part; and

an output buffer part coupled to the capacitor part, and

a second multiplexer part providing the corresponding data lines with the pixel signals from the output buffer part for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal.

2. (Canceled)

3. (Previously Presented) The apparatus according to claim 1, wherein the digital-analog converter part comprises:

a positive digital-analog converter converting the digital pixel data to a positive pixel signal;

a negative digital-analog converter converting the digital pixel data to a negative pixel signal; and

a third multiplexer part selecting one of the positive and the negative pixel signals in accordance with a polarity control signal and providing the selected pixel signal to the demultiplexer part.

4. (Canceled)

5. (Previously Presented) The apparatus according to claim 1, further comprising:

a shift register sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal; and

a latch part sequentially latching the pixel data in response to the sampling signal and simultaneously providing the latched pixel data to the first multiplexer during an enable period of an input source output enable signal.

6. (Canceled)

7. (Original) The apparatus according to claim 1, wherein the first multiplexer and the demultiplexer part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period.

8. (Previously Presented) The apparatus according to claim 1, wherein the sampling part is controlled by an ODD/EVEN signal which performs the time-division on a horizontal period.

9. (Currently Amended) A data driving apparatus for a liquid crystal display device, comprising:

a multiplexer part performing a time-division on ~~inputted~~ input digital pixel data [[on]] for a plurality of data lines for a first horizontal period and providing the time-divided pixel data through a positive polarity output channel and a negative polarity output ~~channels~~ channel;

a digital-analog converter part including:

a positive digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the positive polarity output channel of the multiplexer part into positive pixel data; and

a negative digital-analog converter converting a plurality of time divided pixel data for the first horizontal period provided through the negative polarity output channel of the multiplexer part into negative pixel data;

~~converting the time-divided digital pixel data received from each of the multiplexer part output channels into time-divided analog pixel signals having a polarity corresponding to the polarity of the respective multiplexer output channel;~~

a demultiplexer part separately providing the time-divided pixel signals received from the digital-analog converter to output channels of the demultiplexer corresponding to the data lines, respectively during the first half of a horizontal period and during the second half of the horizontal period; and

an output part outputting simultaneously the pixel signals from the corresponding demultiplexer output channels to the corresponding data lines for a next horizontal period,

wherein the output part comprises:

a sampling part sampling the pixel signals supplied through the output channels of the demultiplexer;

a holding part holding the sampled pixel signals provided through the sampling part; and

a discharging part discharging the pixel signals held in the holding part for a first period to the corresponding data lines for a second period.

10. (Canceled)

11. (Currently Amended) The apparatus according to claim 9, wherein the multiplexer part comprises:

a plurality of positive path switches coupled to input channels for the input pixel data and commonly connected to the positive polarity output ~~channels~~ channel; and

a plurality of negative path switches coupled to the input channels for the pixel data, connected to the positive path switches in parallel, and commonly connected to negative polarity output channel.

12. (Previously Presented) The apparatus according to claim 9, wherein the demultiplexer part comprises:

a plurality of positive path switches forming a plurality of different positive paths corresponding to the data lines, and commonly connected to a positive digital-analog converter; and

a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter, wherein the negative path switches are connected to the positive path switches in parallel.

13. (Canceled)

14. (Previously Presented) The apparatus according to claim 9, wherein the sampling part and the holding part sample and hold the pixel signals supplied for the next horizontal period through the channel different from that of the pixel signal supplied for the first horizontal period.

15. (Previously Presented) The apparatus according to claim 9, wherein the sampling part has a second demultiplexer part comprising:

a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part; and

a plurality of negative path switches forming a plurality of different negative paths and connected to the output channels of the demultiplexer part.

16. (Previously Presented) The apparatus according to claim 15, wherein the holding part comprises:

positive path capacitors charging and holding the positive pixel signals from the positive path switches of the second demultiplexer part; and

negative path capacitors charging and holding the negative pixel signals from the negative path switches of the second demultiplexer part.

17. (Previously Presented) The apparatus according to claim 16, wherein the discharging part comprises:

a second multiplexer part having:

a plurality of positive path switches connected to the positive path switches of the second demultiplexer through the holding part and connected to the data lines; and

a plurality of the negative path switches connected to the negative switches of the second demultiplexer through the holding part and connected to the data.

18. (Previously Presented) The apparatus according to claim 17, wherein the multiplexer, the demultiplexer, and the second demultiplexer are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on the first horizontal period.

19. (Previously Presented) The apparatus according to claim 18, wherein the ODD/EVEN signal performs the time-division on an enable period determined by a source output enable signal for the first horizontal period.

20. (Original) The apparatus according to claim 18, wherein the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal.

21. (Original) The apparatus according to claim 20, wherein the multiplexer part, the demultiplexer part, and the second demultiplexer part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period.

22. (Original) The apparatus according to claim 21, wherein the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part.

23. (Previously Presented) The apparatus according to claim 18, the second multiplexer part is controlled by a second control signal that is phase-inversed with respect to the first control signal.

24. (Previously Presented) The apparatus according to claim 18, further comprising an output buffer part buffering the pixel signals discharged from the holding part to the discharging part.

25. (Original) The apparatus according to claim 24, wherein the output buffer part comprises:

a plurality of positive path output buffers connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and

a plurality of negative path output buffers connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part.

26. (Original) The apparatus according to claim 17, further comprising an output buffer part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines.

27. (Original) The apparatus according to claim 26, the output buffer part comprises:

a plurality of output buffers connected between the output channels of the second multiplexer part and the data lines.

28. (Original) The apparatus according to claim 9, further comprising:

a shift register sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

a latch part latching pixel data and simultaneously providing the multiplexer part with the latched pixel data for the enable period of the input source output enable signal; and

a level shifter part raising a voltage of the pixel data from the multiplexer part to supply the pixel data to the digital-analog convert part.

29. (Original) The apparatus according to claim 17, further comprising a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal.

30. (Previously Presented) A data driving method for a liquid crystal display device, comprising:

performing a time-division on a digital pixel data;

converting the time-divided digital pixel data into time-divided analog pixel signals;

supplying the time-divided analog pixel signals to corresponding output channels;

sampling and holding the time-divided analog pixel signals received through the output channels and simultaneously supplying the held pixel signals to corresponding data lines; and

providing the corresponding data lines with the held pixel signals for an enable period of an input source output enable signal and a reference voltage of liquid crystal cells for a disable period of the input source output enable signal.

31. (Canceled)

32. (Original) The method according to claim 30, wherein the converting the time-divided digital pixel data comprises:

converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and

selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal.

33. (Canceled)

34. (Original) The method according to claim 30, wherein the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time-division on a horizontal period.

35. (Currently Amended) A data driving method for a liquid crystal display device, comprising:

performing a time-division on a digital pixel data and providing the time-divided digital pixel data for a horizontal period through a positive polarity output channel and a negative polarity output ~~channels~~ channel;

converting the time-divided digital pixel data from the positive and negative polarity output channels into analog pixel signals having a polarity corresponding to the polarity of each of the output channels;

separately demultiplexing the time-divided positive and negative analog pixel signals to a plurality of paths corresponding to data lines, respectively during the first half of a horizontal period and during the second half of the horizontal period;

sampling and holding the time-divided analog pixel signals from the paths corresponding to the data lines; and

outputting simultaneously the held pixel signals to the corresponding data lines.

36. (Original) The method according to claim 35, wherein the performing a time-division on a digital pixel data and the converting the time-divided digital pixel data are controlled by an input polarity control signal and a first control signal through an ODD/EVEN signal performing a time-division on a horizontal period.

37. (Original) The method according to claim 36, wherein the ODD/EVEN signal performs a time-division on an enable period determined by a source output enable signal.

38. (Original) The method according to claim 36, wherein the ODD/EVEN signal performs a time-division on a disable signal of a source output enable signal.

39. (Original) The method according to claim 38, wherein the pixel signals are sampled and held by the ODD/EVEN signal for the disable period, wherein the pixel signals in a present enable period are the same as the pixel signals in a previous enable period.

40. (Original) The method according to claim 39, wherein the disable period of the source output enable signal is determined by increasing the disable period of a reference source output enable signal inputted from an external source.

41. (Previously Presented) The method according to claim 36, wherein the outputting the held pixel signals is controlled by a second control signal having a phase inversion with respect to the first signal.

42. (Previously Presented) The method according to claim 35, wherein the performing a time-division on a digital pixel data is carried out by outputting the time-divided pixel data with a polarity through the time-divided pixel data of the output channel opposite to that of the time-divided pixel data and of the output channel for a previous period.

43. (Previously Presented) The method according to claim 35, wherein the performing a time-division on a digital pixel data is carried out by converting the time-divided pixel data into the time-divided pixel data with a polarity opposite to that of the time-divided analog signal and of the output channel of a previous period.

44. (Previously Presented) The method according to claim 35, wherein the sampling and holding the time-divided analog pixel signals is performed by sampling and holding the time-divided pixel signal through a path with a polarity opposite to that of time-divided pixel signal and of the output channel of a previous period.

45. (Original) The method according to claim 35, wherein the output held pixel signals is buffered through an output buffer part prior to supplying to the corresponding data lines, wherein the output buffer part is connected to the corresponding data lines.

46. (Original) The method according to claim 35, wherein the held pixel signals are supplied to the corresponding data lines for the enable period of an input source output enable signal, and a reference voltage of the liquid crystal cells is commonly supplied to the corresponding data lines for the disable period.

47. (Original) The method according to claim 35, further comprising raising a voltage of the time-divided pixel data after the performing a time-division on a digital pixel data.